REMARKS

Applicant thanks the Examiner for indicating that claims 18-28, 31-39 and 41-44 are drawn to the allowable subject matter.

Claims 1-44 are currently pending in the application. By this amendment, claims 1-3, 7, 8, 10, 29-30, and 33 are amended in order to improve claim language. Support for the amendments is provided in at least Figure 24 and at pages 12-15 of the present specification. No new matter is added. Reconsideration of the rejected claims in view of the above amendments and the following remarks is respectfully requested.

The Examiner has objected to claims 3, 8 and 10 for the following informalities: claim 3, line 4 the phrase "said insulator" is unclear whether it is being referred to the layer of insulator or the insulator material of claim 1; claim 8, line 4, the phrase "said insulator" is unclear whether it is being referred to "said insulator material" and claim 10 depends on nonexisting claim 61.

All these informalities were corrected by this amendment. Specifically, Claims 3 and 8 were amended to refer to "said layer of insulator' in order to describe the structure 910 shown in Figures 9 and up and comprises a layer of nitride surrounding the silicon pillar 710. Additionally, responding to the objection claim 10 was amended to properly depend from claim 6. Accordingly, reconsideration and withdrawal of this objection is respectfully requested.

Claims 29, 30 and 40 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, the Examiner states that the phrase "said gate structure is borderless to said second diffusion" is unclear because Figures 23C and 37C shows the gate structure is borderless to the second diffusion. The Examiner also finds that it is unclear how the contact to said second diffusion comprises a spacer self-aligned to said edge described in claim 30. This rejection is respectfully traversed.

Responding to this rejection, as pointed out in the previous response the term "borderless" is used by Applicant to define a such contact opening which can be produced by selective etching at an interface between two materials that can be selectively etched relative to each other. Silicon oxide and silicon nitride can be used as such a pair of materials and can be selectively etched relative to each other. This technique allows formation of an opening in

one of the materials along its interface with the other. If etching is done in accordance with a mask feature of minimum lithographic size and overlapping the interface of the two materials, the opening will be smaller than can be resolved by a lithographic exposure and therefore it is "sub-lithographic" in dimensions. This novel technique allows formation in a convenient manner, extremely small contacts.

The Applicant is respectfully submits that the phrase "said gate structure is borderless to said second diffusion" in Claim 29 describes the structure created by the specific technique described above, which is also described through out the specification and particularly on page 14, lines 16-17.

The Examiner objected the Claim 30 for the reason that it is unclear how the "contact to said second diffusion comprises a spacer self-aligned to said edge". In order to correct claim language and avoid an ambiguity Applicant amends Claim 30. Specifically, claim 30 now reads,

" Claim 30. A transistor as recited in claim 26, wherein said contact to said second diffusion **~~comprises~~** **extends adjacent to** a spacer **which is** self-aligned to said edge."

Additionally, preceding claim 29 was slightly amended to clarify this matter.

The objected by Examiner term "sub-lithographic width" in Claim 40 objected to by the Examiner should be understood as smaller than features as obtained by lithographic exposure which is necessarily limited. By this term Applicant emphasized that proposed borderless structure allows obtaining dimensions smaller than lithography allows. This matter is fully described on page 9, lines 21-23 and on page 3 lines 2-5.

The Examiner objected to the specification as failing to provide proper antecedent basis for the claimed subject matter for several limitations. This objection is respectfully traversed for the reason that pointed out by the Examiner limitations have been described in the specification. Specifically, the phrase "said gate structure extends on at least three sides of said channel" in Claim 23, lines 2-3 is supported by page 12, line 19. Additionally, the phrase "said contact between said first diffusion and said another diffusion extends over insulation between said first transistor and said second transistor" in claim 33, line 2 is presented at page 14, lines 25-32, page 15, lines 1-9 and shown in Figure 23. The language of claim 38, line about "said structure is self-

aligned to said channel" is described at page 12, line 7.

Claims 1-10 were rejected under 35 U.S.C. §102(e) as being clearly anticipated by Alavi et al. (U.S. Patent No. 6,392,271). This rejection is respectfully traversed based on the following discussion.

As it was earlier pointed out the present invention primarily focused on the transistor formation with use of a novel borderless technique, which allows creation of a contact without providing insulation over the structure by forming a contact opening in or along an existing insulator by selective etching. In order to emphasize this feature, by the present amendment claims 1 and 6 have been amended to include the recitation in regard to a borderless element. Specifically, Claim 1 as amended now recites:

not here

"... insulator material in said trenches above said gate electrodes and ~~**adjacent**~~ **between** said sidewalls **and said layer of insulator**, said insulator material being selectively etchable relative to said sidewalls and said semiconductor pillar."

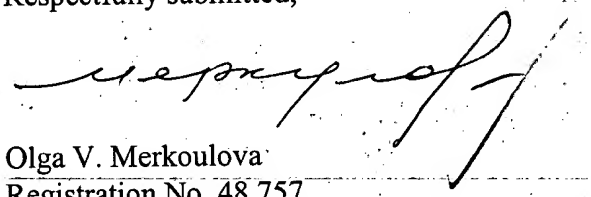
(Emphasis added)

As it was discussed in the previous response, the reference to Alavi et al. does not teach a borderless structure and technique. Alavi et al. shows a vertical MOS transistor, wherein the contact openings are formed by etching in accordance with lithographic patterning of an interlayer dielectric which is different from the Applicant's invention as claimed. It should be noted that Applicant's borderless approach allows contacts with the better dimensional characteristics then a lithography method could provide. Next, Applicant teaches a selective etching of insulator material surrounding gates, while Alavi et al. proposes lithographically etch an ILD (inter-layer-dielectric) layer. Therefore, claim 1 as amended clearly distinguishes over the reference.

In view of the foregoing amendments and remarks, Applicant submits that all of the claims as amended are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue. The Examiner is invited to contact the undersigned at the telephone number listed below, if needed. Applicant hereby makes a written conditional petition for extension of time, if required. Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account

No. 09-0456 of International Business Machines corporation (Burlington).

Respectfully submitted,



Olga V. Merkoulova
Registration No. 48,757

Whitham, Curtis & Christofferson, P.C.
11491 Sunset Hills Road, Suite 340
Reston, VA 20190
Tel. (703) 787-9400
Fax. (703) 787-7557
Customer No.:30743